## CLAIMS

What is claimed is:

1. A signal jitters detection system for detecting jitters of an analog RF (Radio Frequency) signal, which comprises:

a data slicer providing a central level signal for the analog RF signal and using the central level signal to convert the analog RF signal into a data sliced signal;

a data PLL (Phase-Lock Loop) generating a reference pulse;

two A/D (Analog-to-Digital) converter sampling the analog RF signal and the central level signal respectively;

a logic control receiving a trigger of the digital sliced signal to drive the A/D converter to sample signals and outputing a latch signal and a direction signal storing a trigger position of the digital sliced signal;

a memory storing the sample and direction signals of the analog RF signal and the central level signal;

a counter receiving and counting the latch signal of the logic control and outputs the result as an address of the memory; and

a microprocessor controlling inputs, outputs, and actions of the counter, the memory and the A/D converters.

2. The system of claim 1, wherein the trigger position of the digital sliced signal is the

upper end of the digital sliced signal.

3. The system of claim 1, wherein the trigger position of the digital sliced signal is the lower end of the digital sliced signal.

4. The system of claim 1 further comprising a buffer, which sends the sampled signals and the direction signal of the analog RF signal and the central level signal to the memory according to the signal transmitted from the microprocessor and the logic control.

5. A signal jitters detection system using a detector to detect voltage variation of an analog RF signal within a reference pulse period, which comprises:

a data slicer providing a central level signal for the analog RF signal and using the central level signal to convert the analog RF signal into a data sliced signal;

a data PLL (Phase-Lock Loop) generating a reference pulse;

two A/D (Analog-to-Digital) converters sampling the analog RF signal and the sample points are before and after the digital sliced signal triggers;

a logic control, which, after the digital sliced signal is detected to have a trigger, delays a latch signal output by a time unit after a next reference pulse occurs; and

a microprocessor receiving the latch signal and process the sampled signal in the A/D converters.

6. The system of claim 5, wherein the two sample points are separated by one period of the reference pulse.

7. The system of claim 5, wherein the two sample points are separated by one half period of the reference pulse.

8. The system of claim 5, wherein the two sample points are separated by twice the period of the reference pulse.

9. A signal jitter correction method, which comprises the steps of:

setting a range of wander compensation, a range of number of times, and initial values of the wander value and the number of times;

determining the location where signal jitters happen;

computing the signal jitters in a statistical way; and

taking a wander value with the smallest signal jitters within the range of wander compensation as a voltage variation.